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10/619,668	07/15/2003	Dong-Gyu Kim	YOM-0039	7177

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EXAMINER	
PERALTA, GINETTE	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,668	KIM ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-12 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-12 and 20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 9-10, 12, 20-22, 26, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Tagusa et al. (U. S. Pat. 5,986,738).

Regarding claim 1, Tagusa et al. discloses in Figs. 1, 2, 9, and 10 a thin film transistor array panel that comprises a first conductive layer *(32, 62)* formed on an insulating substrate *(31, 61) (as disclosed in col. 9, lines 6-9)*; a gate insulating layer *(33, 63)* on the first conductive layer *(32, 62)*; a semiconductor layer *(34, 64)* on the gate insulating layer *(33, 63)*; a second conductive layer *(37a, 37b, 37a', 37b' in Fig. 2, and 67a, 67b, 67a', 67b' in Fig. 10)* formed at least in part of the semiconductor layer *(34, 64)* and including a data line and a drain electrode *(36b, 66b)* separated from each other *(as shown in Figs. 1 and 9)*, the second conductive layer including a lower film *(37a, 37a', 67a, 67a')* and an upper film *(37b, 37b', 67b, 67b')* of Al *(as disclosed in col. 19, lines 42-46)*; a passivation layer *(38, 68)* covering the semiconductor layer *(34, 64)*; and a third conductive layer *(21, 51)* formed on the second conductive layer and contacting the second conductive layer, wherein at least an edge of the upper film *(37b, 37b', 67b, 67b')*

lies on the lower film *(37a, 37a', 67a, 67a')* such that the lower film *(37a, 37a', 67a, 67a')* includes a first portion exposed out of the upper film *(37b, 37b', 67b, 67b')*, the third conductive layer *(21, 51)* contacts the first portion of the lower film *(37a, 37a', 67a, 67a')*, and at least one portion of a boundary of the semiconductor layer *(34, 64)* substantially coincides with a boundary of the lower film *(37a, 37a', 67a, 67a')*.

Regarding claim 2, Tagusa et al. discloses in Figs. 2 and 10 that an edge of the upper film *(37b, 37b', 67b, 67b')* traverses the lower film *(37a, 37a', 67a, 67a')*.

Regarding claim 3, Tagusa et al. discloses in Figs. 2 and 10, that the passivation layer *(38, 68)* has a contact hole exposing the first portion of the lower layer *(37a, 37a', 67a, 67a')* at least in part, at least a portion of the third conductive layer *(21, 51)* is located on the passivation layer *(38, 68)*; and the edge of the upper film *(37b, 37b', 67b, 67b')* does not coincide with a boundary of the contact hole.

Regarding claim 4, Tagusa et al. discloses in Figs. 2 and 10, that the passivation layer *(38, 68)* contacts the lower film *(37a, 37a', 67a, 67a')* near the contact hole.

Regarding claim 5, Tagusa et al. discloses in col. 19, lines 41-45 that the lower film *(37a, 37a', 67a, 67a')* comprises Cr or Mo.

Regarding claim 6, Tagusa et al. discloses in Figs. 2 and 10, that the array further comprises an ohmic contact *(36a, 36b, 66a, 66b)* interposed between the semiconductor layer *(34, 64)* and the second conductive layer *(37a, 37b, 37a', 37b' in Fig. 2, and 67a, 67b, 67a', 67b' in Fig. 10)*.

Regarding claim 9, Tagusa et al. discloses in col. 9, lines 31-35, and col. 21, line 62 to col. 22, line 5 that the third conductive layer *(21, 51)* comprises ITO.

Regarding claim 10, Tagusa et al. discloses in col. 9, lines 35-37 that the third conductive layer *(21, 51)* comprises a pixel electrode contacting the drain electrode *(36b, 66b)*.

Regarding claim 12, Tagusa et al. discloses in Figs. 2 and 10 that the first portion of the second conductive layer *(37a, 37b, 37a', 37b' in Fig. 2, and 67a, 67b, 67a', 67b' in Fig. 10)* has unevenness.

Regarding claim 20, Tagusa et al. discloses in Figs. 1, 2, 9, and 10 a thin film transistor array panel that comprises a gate conductive layer *(32, 62)* formed on an insulating substrate *(31, 61) (as disclosed in col. 9, lines 6-9)*; a gate insulating layer *(33, 63)* on the gate conductive layer *(32, 62)*; a semiconductor layer *(34, 64)* on the gate insulating layer *(33, 63)*; a data conductive layer *(37a, 37b, 37a', 37b' in Fig. 2, and 67a, 67b, 67a', 67b' in Fig. 10)* formed at least in part of the semiconductor layer *(34, 64)* and including a data line and a drain electrode *(36b, 66b)* separated from each other *(as shown in Figs. 1 and 9)*; a passivation layer *(38, 68)* covering the semiconductor layer *(34, 64)*; and a pixel electrode *(21, 51)* contacting the drain electrode *(36b, 66b)*; wherein a boundary of the semiconductor layer *(34, 64)* is exposed out of the data line except for places near the drain electrode *(36b, 66b)* and an end portion of the data line.

Regarding claim 21, Tagusa et al. discloses in Figs. 2 and 10 that the data conductive layer has a multilayered structure including a lower film *(37a, 37a', 67a, 67a')*

and an upper film *(37b, 37b', 67b, 67b')*, and the lower film and the upper film have different shapes.

Regarding claim 22, Tagusa et al. discloses the second conductive layer including a lower film *(37a, 37a', 67a, 67a')* and an upper film *(37b, 37b', 67b, 67b')* of Al *(as disclosed in col. 19, lines 42-46)*; wherein the lower film and the upper film comprises Ta, Al, Mo, W, or Cr, and Ta is a barrier material.

Regarding claim 26, Tagusa et al. discloses in Figs. 2 and 10 that a lateral side of the data conductive layer *(37a, 37b, 37a', 37b' in Fig. 2, and 67a, 67b, 67a', 67b' in Fig. 10)* is tapered.

Regarding claim 29, Tagusa et al. discloses in Figs. 2 and 10 that the first portion of the drain electrode *(36b, 66b)* contacting the pixel electrode has unevenness.

3. Claims 1, 2, 5-7, 9-11, 20-25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kim (U. S. Pat. 6,087,678),

Regarding claim 1, Kim discloses in Figs. 6 and 15 a thin film transistor array panel that comprises a first conductive layer *(30, 32)* formed on an insulating substrate *200*; a gate insulating layer *34* on the first conductive layer *(30, 32)*; a semiconductor layer *36* on the gate insulating layer *34*; a second conductive layer *(38, 40)* formed at least in part on the semiconductor layer *36* and including a data line *41a* and a drain electrode *41b* separated from each other, the second conductive layer *(38, 40)* including a lower film *38* of barrier metal *(as disclosed in col. 5, lines 19-22)* and an upper film *40* of aluminum (Al) or aluminum alloy *(as disclosed in col. 5, lines 22-25)*; a passivation layer

42 covering the semiconductor layer *36*; and a third conductive layer *44* formed on the second conductive layer *(38, 40)* and contacting the second conductive layer *(38, 40)*; wherein at least an edge of the upper film *40* lies on the lower film *38* such that the lower film *38* includes a first portion exposed out of the upper film *40*, and the third conductive layer *44a* contacts the first portion of the lower film *38*; and at least one portion of a boundary of the semiconductor layer 36 substantially coincides with a boundary of the lower film 38.

Regarding claim 2, Kim discloses in Figs. 6 and 15, that an edge of the upper film *40* traverses the lower film *38*.

Regarding claim 5, Kim discloses in col. 5, lines 19-22 that the lower film *38* comprises chromium (Cr) or molybdenum (Mo).

Regarding claim 6, Kim discloses an ohmic contact interposed between the semiconductor layer *36* and the second conductive layer *(38, 40)*, as disclosed in col. 6, lines 3-13.

Regarding claim 7, Kim discloses in col. 6, lines 3-13 and in Figs. 6 and 15 that the ohmic contact has substantially the same planar shape as the second conductive layer *(38, 40)*.

Regarding claim 9, Kim discloses that the third conductive layer *44* comprises ITO, as disclosed in col. 5, lines 36-48.

Regarding claim 10, Kim discloses in that the third conductive layer *44* comprises a pixel electrode *44a* contacting the drain electrode *41b,* as disclosed in col. 5, lines 36-48 and in Figs. 6 and 15.

Regarding claim 11, Kim discloses in Fig. 15, that the passivation layer *42* has a first contact hole for contact between the drain electrode *41b* and the pixel electrode *44a,* a second contact hole exposing a portion of the first conductive layer *(30, 32) (as shown in the Gate Pad Portion area of the figure),* and a third contact hole exposing a portion of the data line *41a (as shown in the Data Pad Portion of the figure),* and the third conductive layer *44* comprises a first contact assistant *44b* contacting the first conductive layer *(30, 32)* through the second contact hole *(as shown in the Gate Pad Portion)* and a second contact assistant *44c* contacting the data line *41a* through the third contact hole *(as shown in the Data Pad Portion).*

Regarding claim 20, Kim discloses in Figs. 6 and 15 a thin film transistor array panel that comprises a gate conductive layer *(30, 32)* formed on an insulating substrate *(200);* a gate insulating layer *(34)* on the gate conductive layer *(30, 32);* a semiconductor layer *(36)* on the gate insulating layer *(34);* a data conductive layer *(38, 40)* formed at least in part of the semiconductor layer *(36)* and including a data line *41a* and a drain electrode *(41b)* separated from each other *(as shown in Figs. 6 and 15);* a passivation layer *(42)* covering the semiconductor layer *(36);* and a pixel electrode *(44a)* contacting the drain electrode *(41b);* wherein a boundary of the semiconductor layer *(36)* is exposed

out of the data line except for places near the drain electrode *(41b)* and an end portion of the data line.

Regarding claim 21, Kim discloses that the data conductive layer has a multilayered structure including a lower film *38* and an upper film *40*, and the lower film *38* and the upper film *40* have different shapes.

Regarding claim 22, Kim discloses in col. 5, lines 19-25 that the lower film *38* comprises a barrier metal and the upper film *40* comprises an aluminum alloy.

Regarding claim 23, Kim discloses in Figs. 6 and 15 that the data line *41a* has an edge substantially parallel to the semiconductor layer *36*, the edge of the data line *41a* coinciding with an edge of the semiconductor layer *36*.

Regarding claim 24, Kim discloses in Figs. 6 and 15 that the pixel electrode *44a* has an edge overlapping the data conductive layer *(38, 40)* and the semiconductor layer *36*.

Regarding claim 25, Kim discloses an ohmic contact interposed between the semiconductor layer *36* and the second conductive layer *(38, 40)*, and having substantially the same planar shape as the second conductive layer *(38, 40)* as disclosed in col. 6, lines 3-13.

Regarding claim 27, Kim discloses in Fig. 15, that the passivation layer *42* has a first contact hole for contact between the drain electrode *41b* and the pixel electrode *44a*, a second contact hole exposing a portion of the gate conductive layer *(30, 32) (as shown in the Gate Pad Portion area of the figure)*, and a third contact hole exposing a portion of

the data line *41a (as shown in the Data Pad Portion of the figure)*, and the third conductive layer *44* comprises a first contact assistant *44b* contacting the gate conductive layer *(30, 32)* through the second contact hole *(as shown in the Gate Pad Portion)* and a second contact assistant *44c* contacting the data line *41a* through the third contact hole *(as shown in the Data Pad Portion)*, the first and the second contact including the same layer as the pixel electrode.

Regarding claim 28, Kim discloses in Fig. 15 that the passivation layer *42* contacts the lower film *38* near the first contact hole.

Response to Arguments

4. Applicant's arguments filed 7/6/05 have been fully considered but they are not persuasive.

Regarding applicant's argument that claim 1 has been amended to recite that "at least one portion of a boundary of the semiconductor layer substantially coincides with a boundary of the lower film" and that Tagusa discloses in Fig. 2 that the boundary of the semiconductor layer 34 clearly not coincides with either of the transparent conductive (lower) films 37a, 37a', it is noted that in accordance with the applicant's specification and drawings, the coincidence of a boundary of the semiconductor layer with a boundary of the lower film refers to the boundary of each of these films having a surface plane in common as shown in Fig. 2 with the semiconductor layer 154 and the lower film 175p having coinciding boundaries on the plane at the side of the structure, following this Tagusa discloses in Figs. 1, 2, 9 and 10 that the semiconductor layer

(34,64) has a boundary that coincides with a boundary of the lower film (37a, 37a', 67a, 67a') on the plane that is defined by the surface of the substrate.

Regarding applicant's argument that claim 1 has been amended to recite that "at least one portion of a boundary of the semiconductor layer substantially coincides with a boundary of the lower film" and that Kim does not teach that the boundary of the semiconductor layer 36 coincides with the lower film 38, it is noted that in accordance with the applicant's specification and drawings, the coincidence of a boundary of the semiconductor layer with a boundary of the lower film refers to the boundary of each of these films having a surface plane in common as shown in Fig. 2 with the semiconductor layer 154 and the lower film 175p having coinciding boundaries on the plane at the side of the structure, following this Kim discloses in Figs. 6 and 15 that the semiconductor layer 36 has a boundary that coincides with a boundary of the lower film 38 on the plane that is defined by the surface of the layer 34.

Regarding applicant's argument that Tagusa fails to teach the boundary of the semiconductor layer being exposed out of the data line except for places near the drain electrode and an end portion of the data line, it is noted that the boundary of the semiconductor layer 34 is indeed exposed out of the data line except for places near the drain electrode 36b and an end portion of the data line as shown in Figs. 1 and 2 since the semiconductor layer 34 is exposed at a region 24 from the source electrode and the drain electrode.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

ANH D. MAI
PRIMARY EXAMINER